IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,	(	CAUSE NO. 2:21-CV-463-JRG
Plaintiff,	)	
vs.	)	
SAMSUNG ELECTRONICS CO., LTD., et al.,	)	MARSHALL, TEXAS
Defendants.	)	NOVEMBER 4, 2022
	)	9:00 A.M.

MARKMAN HEARING

BEFORE THE HONORABLE ROY PAYNE
UNITED STATES MAGISTRATE JUDGE

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THE COURT: Good morning. Please be seated.

For the record, we're here for the claim construction hearing in Netlist versus Samsung, which is Case No. 2:21-463 on our docket.

Would counsel state their appearances for the record?

MS. TRUELOVE: Good morning, Your Honor. Jennifer Truelove for Plaintiff Netlist. With me today and who will be presenting is Mr. Jason Sheasby, his colleague Annita Zhong, and Michael Tezyan. We also have with us today some corporate representatives, Jayson Sohi, Tobin Hobbs, and Jamie Zheng. We are ready to proceed.

THE COURT: All right. Thank you, Ms. Truelove.

MS. SMITH: Good morning, Your Honor. Melissa Smith on behalf of SamSUNG. I'm joined this morning by Mr. Mike McKeon, Mr. Matt Colvin, Dr. Frank Albert, Mr. Jeff Burton. And then, Your Honor, we also have two corporate representatives from Samsung today--Young-Jun Choi, as well as Won-Jin Lee. And Your Honor, we're ready to proceed.

THE COURT: All right. Thank you, Ms. Smith.

I will also point out for the record that earlier this morning we distributed to counsel for both sides a set of preliminary constructions of the disputed terms. The purpose of issuing those preliminary constructions is not to deter either side from taking whatever positions they think are appropriate on these terms; rather, the preliminary

constructions are designed to let you know where the Court is after the initial review of the briefing and the record so that you can focus your arguments where you think the Court may have most gone astray. I do reserve the right to amend these preliminary constructions, and not uncommonly do alter them based on the arguments received at this hearing, so I hope that you will take them in that spirit.

I'd like to hear the arguments on a term-by-term basis, but I'm happy to take them in whatever order counsel think is most productive and to group them if counsel think that would be efficient.

And I will note also that a variety of these preliminary constructions have notes on them. Those notes are not part of the official construction; they're designed to let you know what will be reflected in the order that issues so that even though it might say 'plain and ordinary meaning', there will be further discussion in the order that issues designed to govern the way the experts handle these terms. So I just wanted to let you know that's what those parenthetical notes are intended to communicate.

Having said that, I'll turn it over first to counsel for Plaintiff.

Good morning, Mr. Sheasby.

MR. SHEASBY: Good morning, Your Honor. May it please the Court.

On term A, we will stand on the papers because the Court has preliminarily adopted our construction, and perhaps Samsung would appreciate the opportunity to argue on that one.

THE COURT: All right.

MR. McKEON: Good morning. Mike McKeon for Samsung. Always a pleasure to appear before you.

So I do want to make just a few points on the first term, the 'dual buck converter' term. And one thing I want to emphasize, and maybe we didn't do as good a job in our brief as we should have in this, but this term 'dual buck converter' that appears in dependent claims, it shows here on slide 7 a depiction of what that physically looks like in the patent and it's depicted in figure 16.

This term is not a term of art--'dual buck converter'. 'Buck converter' is. That's why no one's disputing that term. But 'dual buck converter' doesn't have a common, ordinary, understood meaning, and that's why, you know, we think it's appropriate in this case to look to the specification to get guidance on that. And when you do that, what you see here is in figure 16 and the corresponding description at column 29 of the patent, starting at line 46, which really defines and gives meaning to what this term, which has no understood meaning in the art, what it means in the context of the patent. And what we see here is that when we talk about the dual buck converter, we have these two voltages coming out.

No one, of course, disputes that. It's two voltages coming out. But one voltage that comes out is different, distinct from the other voltage comes out.

And the explanation here in the patent is -- again, at column 29, is that you have the 2.5 voltage coming out, and in the context of the embodiment, it's going to a particular device in the whole system, an isolation device; whereas, the second voltage is a reduced voltage, and that's going to the -- a separate and distinct device--FPGA. And so we have these two voltages coming out, but the voltages are different.

And, in fact, if we go to slide 9 here in our presentation, what we see here if you look at all the buck converters, they all actually have different values at the output. And why is that? Because the patent describes in quite detail that we want to drive different types of components in the system, and these different components are going to have different voltage requirements. And the logic here, Your Honor, is, Well, if I had two components that only needed 1.8 volts, well, then I just need one output of a buck converter that I can send to both of those components. So I don't need -- if I have a buck converter with a dual output, it would be superfluous, completely redundant, unnecessary to have them be the same voltage.

And we see the descriptions in the specification here at column 29, you know, quoting here at line 33, you know, "an

appropriate amount of powering for the various components." And the way the system is defined in the patent, and particularly the buck converters, in every instance -- there's not a single instance where we have a different value or a same value coming out not only within the dual buck converter, but actually across the buck converters, because again, that would be superfluous; you wouldn't need to do that.

One final point, Your Honor, is there is a claim in the patent where we talk about a first and third buck converters are configured to operate as a dual buck converter, and the point here is that when -- if I had these separate buck converters that had these separate values in the independent claim and I bring them together in the dependent claim, then they're going to have -- retain their separate values and -- when they're combined as a dual buck converter. And again, it -- you know, it would make no sense as a matter of logic or as a matter of the technology as described in this patent to have them be the same value because you would just have one output then that would go to the different components.

THE COURT: You know, Mr. McKeon, that sounds like a good argument to me for the system having the capability to have a different value out of each buck converter, but where do you derive a requirement that it can only be different values?

MR. McKEON: I would say, Your Honor, when the

disclosure is limiting in that way, when THE -- to describe the embodiment -- and again, this is not a term of art. When they describe 'dual buck converter' in the patent, it's only described this way. And I do concede, Your Honor, looking at the claim language itself, you know, if you want to take the most broadest view of the claim language itself, your proposed construction in the preliminary is, you know, within that logic. But if you look at the specification and one of ordinary skill in the art is thinking, What about the dual buck converter, I'm going to have to go to the specification, and when you have it consistently and uniquely defined in this way, then, you know, we think that's limiting, and that's really the source of our point here, our argument here.

THE COURT: You know, I would quibble with your use of the word 'defined'. I don't see it defined in the specification at all.

MR. McKEON: What I would say, Your Honor, we rely on cases like *Bell Atlantic* where you have these -- you know, defined by implication. You're absolutely right, Your Honor; it's not defined in the sense that 'dual buck converter' is herein defined as X, Y, and Z, and that's definitely the case, Your Honor. But when you have a description of a component that has no ordinary meaning in the art and it's the only description of it, then you have to define it by implication, and we think that's really what's going on here in the context

of this term.

THE COURT: And let me back up and question a premise you have on the screen right now, which is that the first buck converter and the third buck converter must involve different voltage amplitudes. Is that just an implicit characteristic as you see it, or is there something in the specification that you think requires that?

MR. McKEON: Again, Your Honor, going back to the -- sort of the main foundation of our argument, which is the only disclosure is that they have -- all have separate values coming out. And again, it would be superfluous if I was to have -- if these were all the same values, to be superfluous you would just need one output and you could drive as many different components in the system as you wanted to with that one value. The point is that these difference components that are in the system require different values.

And that is why we have these -- you know, you have these -- this one voltage coming into all these buck converters, you have one voltage coming in at 1110 or, alternatively, 1112. That's value coming in. One value is coming in. And these different buck converters are going to downscale that value, it's actually five volts coming in, and they're each going to down-tick the value to the appropriate level and they're all going to have different values. And if you had a system where they could be the same, then you wouldn't need these different

buck converters.

And we just think with the term 'dual buck converter', particularly because it's not defined in the art, you know, you're going to have to be stuck with you what you disclosed to the public in your patent. And that's the main point and premise of the argument, Your Honor.

THE COURT: All right. Thank you, Mr. McKeon.

MS. SMITH: Your Honor, may I pass up some slides, please?

THE COURT: Sure.

MS. SMITH: Thank you.

THE COURT: Thank you, Ms. Smith.

Go ahead Mr. Sheasby.

MR. SHEASBY: Thank you, Your Honor.

I think the basic premise of the argument is that two separate components cannot demand the same value on the module, and that is absolutely inconsistent with the patent. This is the '918 Patent, 29, 18 through 64, and this is an object lesson in why there may be lots of reasons to have separate circuits delivering the same voltage.

So in this example the DRAM, flash, and controller all require 1.8 volts, and there is an option of them being supplied over a single line, 1102. But then if you go down to the bottom of that same passage, it makes clear that an independent voltage can be used to supply the DRAM and flash.

And, of course, those DRAM and flashes still require the same 1.8 volts; they're just being supplied independently. And so the basic premise that each of the wires has to, in effect, supply a different voltage is not in the specification itself.

The dual buck converter, there is no evidence that that's a specialized term of art or a term that was coined by the patent owner in this case. The purpose of the figure 16 embodiment is to note that you can use lots of different types of power management tools. You can use buck converters, you can use dual buck converters, you can use buck and burst converters, but there's no requirement or -- there's no requirement or standard that each of those has to deliver a different voltage. For example, we know in the preferred embodiment that the voltage 1122 is outputting 1.8 volts, but, in the alternative, there can be a separate for DRAMs, flash, and FPGA, but we know in the alternative embodiment there could be an independent voltage.

Thank you, Your Honor.

THE COURT: And Mr. Sheasby, is there a reason that you can articulate why a dual buck converter would have the same voltage coming out on both lines?

MR. SHEASBY: There is, Your Honor, and I can explain it. There is two reasons.

If you go to slide 66.

In particular in FPGA--and you can look at this from the

specification itself--the FPGA operates not just at one voltage; it can operate at multiple voltages at different particular times. And that's talked about in the specification. If you ran the core of the FPGA, you would operate at one voltage; if you ran other elements of the FPGA, you'd operate at another voltage. And so, for example, this is talking about FPGAs that operate across voltage ranges that start from 1 and go up to 2.5 volts.

And so the reason for the dual buck converter having the capability of doing different voltages, but not requirement, is that it's not an assumption that the voltage demand for a given component will stay the same throughout the operating cycle. And the specification in particular talks about the FPGA operating at different voltages in different events.

THE COURT: All right.

MR. SHEASBY: Thank you, Your Honor.

THE COURT: Thank you, Mr. Sheasby.

MR. McKEON: Your Honor, I think you got the argument, so with that, we rest.

THE COURT: All right, then. Thank you, Mr. McKeon.

And we can take the next term.

MR. SHEASBY: Your Honor, I think for B, C, and D we will stand on our briefing.

THE COURT: All right.

MR. McKEON: Ms. Andrews, can we have the slides?

All right. 'Pre-regulated input voltage', Your Honor. So, I mean, the dispute here, of course, as Your Honor knows reviewing the briefs is, you know, whether this regulated voltage needs to be generated on the memory module itself. That's really the crux of the dispute here. And, you know, I'll note that their proposal, of course, modulated input voltage. And the thing about their proposal, Your Honor, it takes out the word 'pre-regulated'. 'Pre-regulated' must mean something. You know, 'pre-regulated input voltage'. And if you just say 'modulated input voltage', what does that -- that really changes the character of what 'pre-regulated input voltage' is.

And we think from the context of the disclosure in the patent, and also the claims, is that the pre-regulated voltage, it comes from the input voltage, the source of it, but the key is that it's actually done on the module. And, of course, the pre-regulated voltages serve to be an input into the buck converters we just talked about.

And this is where the language appears in the claim. And just take a second, Your Honor, if I can, to walk through -- sort of piece together how the claim operates in these different elements. Of course, we have that printed circuit board. And we had this input voltage. That comes in and that is going to this power element. And the power element is what is generating on the actual module, on the circuit board, it's

generating the pre-regulated input voltage which, in turn, goes to the buck converters and, of course, is an output and that goes to another component. So the patent is very clear in its description how these all relate, and we -- you know, we think the claim is very consistent with that.

And the disclosure here, Your Honor, is also very clear on this. And what we've highlighted here in this red, these are the two power elements, and both take that input in and what they're doing is they're cranking that up to a higher level and they're pre-regulating the voltage. And what are they pre-regulating the voltage for? Well, they're pre-regulating it to be inputs into the buck converters we talked about. And then the buck converters, in turn, will down -- you know, down shift the voltage. But the pre-regulated voltage is something that's generated on the power module because it's tied directly to the buck converters. They're the inputs to the buck converters. And, of course, we see that in the disclosure how they're all tied together.

Now, there's an argument made by our capable counsel here on the other side about figure 12, and I just want to quickly respond to that. Now, figure 12 is a different configuration, and then what I have here on the slide is figure 12 and this power source 1080. And the argument that was made is, Well, what if you take the figure 12 power source

and you could bring it into figure 16. And there is disclosure in the patent that says that, but it has nothing to do with the pre-regulation. I mean, the figure 12 doesn't even talk about pre-regulated voltage.

And the reason why counsel points out figure 12 is because there is actually a section in connection with describing figure 12 that says 1080, this power source, can be off the module. It says that for figure 12. And they cite to that and say, Okay, Your Honor, therefore, you shouldn't have that requirement. But Your Honor, I think the point there is that actually the fact that it says it for figure 12 and does not say it for figure 16 I think is quite telling. I mean, they -- when they want to have clarity around where these different components could be and where these signals are generated, they gave you the option of figure 12, but they specifically did not do that in figure 16.

And figure 16, of course, is very important because that's where the pre-regulated voltage term is applicable. The pre-regulated voltage is the green here on the right, and that's coming from the power sources, and it's generated on the board, and it's tied directly to the buck converters. And the way they've construed it, Your Honor, and I fear the way that your preliminary -- the scope of your preliminary is that, you know, this pre-regulated voltage can be generated, you know, systems away, and as long as it ends up into the

buck converters that's all that matters. And we just think, Your Honor, that's a step too far given the context of this term as it's used in the patent, and also, you know, the pre-regulation. That's a term in the claim. And I fear, Your Honor, that your construction just removes that. And what meaning does that have in the context of this claim and this patent--pre-regulated voltage. And we feel, Your Honor, that, you know, it's got to be tied directly to those buck converters and it's got to be generated on the module.

And with that, Your Honor, I'll save --

THE COURT: I guess my initial read on this is that while pre-regulated voltage is a limitation of the claim that has to be met, the claim as it's written is agnostic as to where that occurs. And I understand that there is an embodiment which is displayed in figure 16 that would support your understanding of it, but my difficulty is in finding that that embodiment has to be read into the claim.

MR. McKEON: And Your Honor, that's obviously a great question, and what I would say to that is, you know, again, I would just -- I would hang my hooks onto that 'pre-regulated' term. But if you look at the way the claims set up, you've got this input voltage coming in and it's coming in from these edge connections, and the edge connections are on the module. So I have the input voltage coming from the edge connections and then I'm generating these

pre-regulated input voltages. They're pre-regulated input voltages, and these input voltages, where do they come from? They don't just fall from the sky. They came in through the edge connection. So the input voltages are on the board. And when they make the pre-regulated input voltages, I'm doing that on the board because they're coming from what came in through the edge connection.

So I think the claim itself really gives you the structure of how these voltages are related, and it's tied directly back to figure 16. So they're coming in from the edge. That's a structural limitation there. The input voltages are coming into the edge, and then they go into the power circuit, and they are pre-regulated, and that's all on the board. And, you know, the pre-regulated input voltages, again, they are not just falling from the sky; they're coming -- they're generated on the board, and the source of them, you know, is what's coming into those edge connections. That's the source of that power. And so the claim itself is what really puts that structure together there, and I think, you know, when you look at the patent it really brings it home.

THE COURT: All right.

MR. McKEON: Thank you, Your Honor.

THE COURT: Thank you, Mr. McKeon.

MS. ZHONG: Can we switch? Thank you very much.

THE COURT: And Ms. Zhong, if you can pull that mic

down to you. I want to make sure I can hear you. Thank you.

MS. ZHONG: Can you hear me now?

THE COURT: Yes.

MS. ZHONG: Thank you, Your Honor.

So why don't we start with slide No. 72.

Let's start with the claim language. And Your Honor has pointed out there is really no connection between the pre-regulated input voltage and the input voltage that's received from the edge connection. As Samsung's counsel has pointed out, the pre-regulated input voltage is an input for the buck converters, and there is a separate input voltage from the portion received at the edge connections. The claim otherwise does not place any restrictions on the two terms.

And then if we go to figure 16 that the counsel has hang its hat on, if you look at figure 16, it's not a memory module. What it says is a power module. The power module can be part of the memory module or it can be off the memory module. So think about when it's off the module there is a memory module, there is a separate connector where the power module is actually connected to the memory module. So figure 16, the caption of it, the description in column 9, lines 39 to 41, says figure 16 is a power module illustrating a power module. It's not illustrating the memory module. That power module can be part of the memory module as shown in, for example, figure 12, 13, and 14 illustrated on the same PCB, or

as described in the specification for figure 12, it can be off module.

So Your Honor got it right--the pre-regulated voltage need not be generated on the same PCB as the memory. They can be off module. The patent the inventors anticipated and described both possibilities, and that's in, for example, column 26, lines 26 through 35.

So in column 26 through 35, they contemplated both having the second power module 1080 on the same PCB as a memory module as the rest of the memory or it's to be off. And the power module is exactly the same.

If Your Honor doesn't have any additional questions, we will rest on the paper at this time.

THE COURT: All right. Thank you, Ms. Zhong.

MR. McKEON: Your Honor, a quick response to that?

THE COURT: Certainly.

MR. McKEON: And again, Your Honor, I just want to emphasize, the description regarding having the power module, you know, removed from the memory module, that's in column 26 with connection with figure 12, and then -- and counsel cited that, you know, being at line 30. And the point is that description does not appear anywhere in connection with figure 16, and the claims here are clearly directed at figure 16. If you're talking about buck converters and all that, that's figure 16. That's -- the only disclosure of the system is

figure 16. And the fact that that same description that counsel pointed to is not anywhere near figure 16 description really tells -- I think tells the reader and one of ordinary skill in the art that this is a different configuration of figure 12. And with respect to figure 16 description, what the claim corresponds to, these are done on the module. And again, the word -- the 'pre-regulated' language I think supports that.

With that, Your Honor, unless you have any questions, we can turn to the next term.

THE COURT: All right. Thank you, Mr. McKeon.

MR. SHEASBY: Mr. McKeon, I already said I was going to rest on -- just to make it more efficient, the next three I'm going to rest on.

MR. McKEON: Thank you.

THE COURT: All right. So I'll hear from the Defendant on anything on the C and D terms.

MR. McKEON: Thank you.

On this one, Your Honor, if I may -- so 'first', 'second', 'third', and 'fourth'. And I think the issue here, Your Honor, is what is 'distinct'. And as Your Honor -- you know, the case law is clear that, you know, these need to be distinct. So we're having an issue about what is 'distinct'. And I think, you know, were -- the construction, as Your Honor put in the preliminary, 'distinct' is just physically

separate; it's distinct, and in our -- we're going further than that; we're saying yes, you've got to have that, but you also -- in the context of this patent and this art, 'distinct' also needs to be distinct in value. So, you know, separate and then distinct in terms of the values.

And on this point, Your Honor, there's a case *Alexsam*/*Cigna* case that we cite in the brief, and the issue there was the first database distinct from the second database. And this is one of your decisions, Your Honor. And what you held there, you know, you held they have to be distinct consistent with the case law, but then you said, you know, you're not going to get into the issue about what that means in the context of that dispute. You felt that was something the jury should decide. And what we would invite here, Your Honor, is this same result. Let 'distinct' -- we all agree they have to be distinct, and there's no dispute about that. And what we would invite, Your Honor, is sort of following the logic of the *Alexsam* case and let's let the jury decide the context of this patent and technology--you know, what does it mean to be distinct. And I think that's something that our experts are going to get up there and talk about and that's something that the jury can ultimately decide in the context of this technology and this patent.

THE COURT: You know, in the *Alexsam* case, what we were concerned about was the issue there you have a single

database and one side wants to draw lines and partition it into allegedly multiple databases, and that was the fact issue that was involved with whether they were distinct. I don't see that there's a similar issue here with these first through fourth voltages, but --

MR. McKEON: Yeah. I mean, I guess, Your Honor, the -- I mean, I would say the logic applies equally and, you know, so I get the line-drawing point is it a distinct debate as different in nature, but fundamentally, you know, whether the voltages first, second, and third are distinct in the context of this technology, you know, ultimately that's the question at hand here, and I think that was -- I think that's best left to the jury in this context, following the same logic.

THE COURT: Well, I just wanted to make sure that it was clear that the position that I'm taking at this point is that you are right, they have to be distinct, but I'm not agreeing that being distinct means they have to have different amplitudes, and that's what I guess to a certain extent you were talking about before. I understand that may be the highest and best use of this system, but the question is do the claims require it, and that's what I'm struggling with.

MR. McKEON: Yeah. And I -- that is certainly the debate, Your Honor, and that's why, you know, I invite the Court to, you know, use the same logic that you did in the

Alexsam case here and let the jury decide whether in this context what we see here on slide 16 and whether these are distinct, you know, in the context of an accused system or not, and let that just -- the jury decide that ultimately, and leave it at distinct, that will be part of the construction, and then the jury can take it from there.

THE COURT: All right. I understand the argument.

MR. McKEON: Thank you, Your Honor.

THE COURT: Thank you, Mr. McKeon.

MR. SHEASBY: So we start with the claim language the Federal Circuit requires. If you look at the claims, it recites one or more regulated voltages, so multiple regulated voltages through the fourth. And then -- that's claim 23 of the '918. And then in dependent claim 29 it makes clear that those regulated voltages can actually have the same amount.

THE COURT: Mr. Sheasby, you're a bit taller than your co-counsel. If you could adjust that mic that would help. Thank you.

MR. SHEASBY: Not in personality, Your Honor; only in height.

You asked this question, which is why would two separate lines give the same voltage, and I gave you one example from the specification that the FPGA operates in different states and, therefore, requires different voltages. There's another example. So if you look at this specification '918, 29, 18

through 64, it talks about the wire, the rail for the voltage being provided at 1.8 volts for two amps for 60 seconds. And, of course, what we know from electrical engineering is that voltage is only one aspect of what triggers the load that's placed on a circuit.

So the analogy that Doctor Zhong gave to me yesterday was the following: There's a reason why you don't plug in a power strip and plug in four microwaves all at 110 volts into the same circuit, and the reason for that is that you'll short the circuit because the load will be too great. And what this passage is speaking about is the fact that one circuit--this is 1122--is going to provide 1.8 volts, but it's going to provide it two amps for 60 seconds. But you may need the same voltage but different amps and a different load for another circuit, and that's why the specification expressly describes the voltages as being able to be independent even though they're the same amount, because voltage is only one of the three parameters that describe how you feed the modules that you're dealing where.

If you go to slide 57.

This is another example that we look at. This is from --

Slide 56.

This is from PNC -- from Samsung's own papers. This is Exhibit 30 to our reply at papers 15 and 30. And they

acknowledge this as well, that separate voltages can have the same amplitudes.

So this is I don't think anything esoteric or funny. This is a basic element of electrical engineering, which is that you may want different rails or different pipes all differing the same voltages because voltage is only one of the parameters that is contributing to the load you need to feed from those circuits.

I'll rest on that, Your Honor, unless you have any questions.

THE COURT: All right. Thank you, Mr. Sheasby.

MR. SHEASBY: Thank you, Your Honor.

MR. McKEON: Just a brief response, Your Honor?

THE COURT: Certainly.

MR. McKEON: Just for the record, and we do take issue with the description that the specification discloses using the same voltage in these different components and, you know, Mr. Sheasby pointed to some extrinsic evidence Samsung documents regarding how their systems -- well, I guess it's a JESD bag. But the point is in the specification there's no disclosure of that in the specification.

THE COURT: Well, I guess the question is, what I understand from the Plaintiff's argument is that they're saying that's a reason why it would make sense for the capability to have different voltages but not a requirement.

And if you want to rebut the argument that it would be useful to be able to have the same voltages from the different circuits, then tell me about it, but that is what I'm struggling with--just because the embodiment shows separate voltages, does that make it a limitation.

MR. McKEON: And I would say yes, Your Honor, in this context. I mean, again, there is just no disclosure where you have it -- they'd have the -- they would be the same. And then, of course, in the context of the patent, where you have these various buck converters, they're going to different places, and there's no disclosure that you would have -- that a particular FPGA in one system would have the same voltage as an FPGA in another part of the system. There's no disclosure on that. And yes, you can have different FPGAs, but there's no disclosure that they would necessarily have the same voltage.

And maybe in a real-world system you would have situations where that would be the case, but we're limited to what we've got here in the patent documents. And when you have this disclosure that's very specific in terms of the different values of these signals and nothing else, then, you know, we think that's limiting.

THE COURT: All right. I do understand the argument. Thank you.

MR. McKEON: Thank you, Your Honor.

MR. SHEASBY: Your Honor, we'll rest on -- I think I just referred Your Honor to the passage 29, 33 through 64 which talks about a flash and DRAM, two separate components both at 1.8 volts, and we disclosed them being fed by separate independent lines.

And with that, as to term E we'll rest as well, if my brother would like to argue that in the first instance.

Term E. Did you want to argue term E?

MR. McKEON: Your Honor, we're going to rest for D, E, and F. We will rest on the papers.

MR. SHEASBY: So with Your Honor's permission, we will argue F.

THE COURT: All right. Go ahead.

MR. SHEASBY: Thank you, Your Honor.

MS. ZHONG: Slide No. 80, please.

It's our position that the memory module should be limiting because it provides the antecedent basis for the test in the body. That's consistent throughout the claims. For example, claim No. 1, the preamble says a memory module, and that provides the antecedent basis for the end of the memory module at the end of the first limitation. There is well-established case law that says if the -- a term that's appearing in the preamble provides the antecedent basis for the text in the body, then that particular phrase should be considered unlimiting.

And with that I will rest.

THE COURT: You know, it can be limiting because it provides antecedent basis, but this certainly looks like nothing more than a statement of an intended use of the device. Does it provide any other meaning to it other than the intended use?

MS. ZHONG: Well, it requires -- if Your Honor looks at --

Let's go back to claim No. -- slide 81.

The first limitation is, A printed circuit board having interface configured to fit into a slot, and that interface is required to include a plurality of edge connections, to couple power, data, address and control signals between the memory module and the host system. So that provides a context.

There is an interface -- think about the DEM. There is a bunch of gold fingers on the edge. And that gold edge, those gold fingers are supposed to provide power data and control signals between the host and that memory module, like the DEM board. So it provides a context of it--what is that interface coupling. So the memory module provides that context. It's not an intended use. It provides -- defines a physical structure where the interface needs to couple the signals with.

THE COURT: So you're saying without the preamble being limiting, it does not -- the claim does not define a

complete apparatus?

MS. ZHONG: Well, it makes clear that the printed circuit board -- the interface on that printed circuit board is providing the -- is coupling the signals between the host and that system. So everything else -- for example, the voltage conversion, the plurality of the component coupled to that is part of the memory module between which -- and the host system the interface is providing the conduit, or like the pass way for the signals. So it does provide the context.

THE COURT: So you're saying that if we don't construe the preamble as limiting, the claim will not be clear as to what the -- whether the device is the memory module that's referred to at the end of the first limitation?

MS. ZHONG: That's correct. For example, whether the voltage conversion circuit needs to be part of the memory module or not, then it's not going to be clear.

THE COURT: All right. Thank you, Ms. Zhong.

MR. McKEON: Okay. All right. So Your Honor, just where you started, I mean, this really is intended use. The point is here you have this printed circuit board, and the printed circuit board is doing various things and it's just doing this coupling between these other things. These other things aren't part of -- it doesn't indicate here specifically that they're part of what the printed circuit board is doing.

And I think the case that we think is on point here, Your

Honor, is, you know, your ruling in the *Sol IP* case where we had the same situation where we had a reference to the wireless communication system that was in the preamble, and Your Honor, you know, the same logic really that applies here is that it really doesn't overcome that presumption that, you know, it's not limiting. And you don't -- it's not really part of the claim and part of the system that's claimed. Even though it is, in fact, referenced, you know, within the body of the claim, it's not really doing anything, and particularly in the case we have here which is really an intended use situation.

THE COURT: Well, the argument I'm hearing from the Plaintiff is that it may not be clear that the memory module identified at the end of the first limitation is the device itself, the claimed device. Do you believe that it is clear that the memory module within the first limitation is the overall device even if the preamble is not limiting?

MR. McKEON: Well, I think what's required is that the printed circuit board do these things. Right? It has the plurality of edge connections configured to couple power, data, and address and control signals. And the point there is the coupling that it's performing, this thing you hold in your hand, the coupling it's performing is between the memory module and the host system.

And, you know, the host system here has no antecedent

either. I mean, it doesn't --- I mean, that particular term doesn't have any antecedent. The point, though, is -- well, I guess it does. I take that back, Your Honor. It's up in the other -- in the top here.

But the point is that these two separate modules and the system for the host system, they're outside of what we're talking about here. And the only thing that the printed circuit board is doing, it's making sure that these power, data, address and control signals, that it's coupling between these two systems. And so I don't --

THE COURT: Well, the PCB that's claimed in the first limitation is claimed as part of the memory module, isn't it?

MR. McKEON: Well, it's a comprising term. Right? So it would include -- you know, it would include memory -- the memory module will have a PCB, a voltage conversion circuit, and a plurality of components. That's how you'd read the claim, for sure.

THE COURT: Well, I guess what I'm hearing from the Plaintiff is the concern that if the preamble is not limiting, that first limitation could be read as referring to a memory module that is not part of the device that's claimed; that it is just referring to a connection between some unclaimed device, the memory module, and the host system.

MR. McKEON: I -- yeah, Your Honor. I don't -- I

guess I don't agree with the argument. I mean, the point is here you have the memory module, and it's not like the antecedent goes away and is irrelevant. You know, it still guides your -- how this claim operates. It's clearly -- the memory module that is at issue here is the one that the printed circuit board is sitting on, but doesn't mean -- it doesn't mean that all of the sudden the memory module is a requirement of the claim. It's just saying that between the memory module that the printed circuit board is sitting on and the host system, that's where these -- this connection is occurring, between those two things.

THE COURT: What difference do you see it would make if we construe the preamble as limiting?

MR. McKEON: Well, I mean, in terms of how it impacts the case, Your Honor, I -- you know, it's not clear the scope of the impact that it would have. But, you know, for just ordinary rules of claim construction here, I think this is a situation where we wouldn't want that to be limiting based on the fact that this is really, you know, an intended use situation. And despite the fact that the memory module is referenced in the text of the body of the claim, you know, it's not limiting in the context here.

THE COURT: I guess what I'm going to have to figure out is whether I think that the preamble gives life or meaning to the claim in view of the argument that the memory module in

the limitation could be understood to be something other than the claimed device. But anyway, I'll -- I will look at that further.

MR. McKEON: Okay. Thank you, Your Honor.

THE COURT: Thank you, Mr. McKeon.

MS. ZHONG: Your Honor, just one clarification. The reason we want to make sure that the memory module is limiting is to make sure that each of the claimed elements, printed circuit board, voltage conversion circuit, and a plurality of the components, we want to make sure these are all part of the memory module. Without that, there could be confusion. And it doesn't seem that Samsung's counsel disagrees with it. We want that. We just want the clarity so there is no argument down the road.

THE COURT: All right. I understand that position. Thank you.

That takes us to the 'array die' term.

And I can tell you, Mr. Sheasby, that the basis of this construction is the prosecution history disclaimer argument, in case that wasn't clear.

MR. SHEASBY: Understood, Your Honor. And let me go straight there.

So this is the passage from the prosecution history, and it does, indeed, say that Rajan merely discloses DRAM circuits 206A through D, which are different from the array dies. And

I understand that Your Honor has concluded that that is a disclaimer. The issue that I have is that -- we understand that -- does Your Honor intend to give anymore guidance as to what the DRAM circuits are that is excluded, or will that be for the experts to analyze?

THE COURT: That would be for the experts. I do not intend to try and define what DRAM circuits that are disclaimed.

MR. SHEASBY: I understand, Your Honor.

With that clarification, there's no need for any additional argument. Thank you, Your Honor.

THE COURT: All right. Thank you.

MR. COLVIN: Your Honor, Samsung will rest on the papers for that term as well.

THE COURT: All right. Thank you, Mr. Colvin.

MR. SHEASBY: Your Honor, we will rest as to H on the papers.

THE COURT: All right.

MR. COLVIN: Samsung will also rest on the papers, Your Honor.

THE COURT: Thank you, Mr. Colvin.

MR. SHEASBY: And I believe that I, J, and K are all the adoption of our positions, and so if Samsung wants to argue those I'll allow them, obviously. So we don't have to jump up so often. I won't allow you to do anything. You can

do whatever you want. My point is that I won't sit up here, and let you guys do what you want.

THE COURT: All right.

Doctor Albert.

DOCTOR ALBERT: Good morning, Your Honor. Frank Albert for Samsung.

The first term here, term I, 'before receiving the input C/A signals corresponding to the memory read operation', and Samsung's proposed construction is 'during one or more previous memory operations'. What we believe is this provides clarity to the term, it is based on admissions made by Netlist during the prosecution, as well as the clarity provided by the specification.

Let's take a look at the claim here. So the highlighted portion here is the actual claim language that we're discussing, 'before receiving the input C/A signals corresponding to the memory read operations at the module control device'. It's 'before receiving' that is the thrust of the attention here. That portion of the claim relates back to an earlier part of the claim, 'receiving at the module control device input C/A signals corresponding to the memory read operation'.

The second half of the construction, the thrust of the discussion here is determining the first pre-determined amount based at least on signals received at the first data buffer.

So really the question is when is it linked between -- when is it that determining the pre-determined amount, when does it actually happen; what does 'before receiving the input signals corresponding to the memory read operation at the memory module' mean in the context of this claim, this patent, this prosecution history.

So if you look to the patent, figure 18 provides a good illustration of that. We start off with steps 1810 and 1820. There's a previous write operation. You can see that in 1820--'receiving a write strobe signal'. And then based on that previous memory operation, a pre-determined amount of delay is generated. It says right there in 1830, 'generating a delay signal according to the time interval'.

Now, later on when we receive a read signal in 1860 and 1870, that read signal, there's going to be a delay in the read strobe here at 1880 based on that pre-determined amount that was determined earlier during that previous memory operation.

Now, if you look to the specification, over and over and over again is the determining that pre-determined amount that's linked to that previous memory operation. Here we have some examples. Patent -- '506 Patent at 4, 9 to 19, single alignment circuits that determine during the write operation the time interval. Again, the time interval is used during subsequent read operation to time transmission of the read

data to the memory controller. Another example --

THE COURT: Mr. Albert, the passage that you just read starts with "Further, in one embodiment". Why should I take that as a limitation?

DOCTOR ALBERT: It's not just this embodiment, Your Honor. It's over and over and over again in the patent. And if you look to the prosecution history as well, they actually explain, further explain what this means. So let me -- I could fly by these other slides, Your Honor. These are just additional examples of time and time again where the patent talks about determining that time, that delay time based on the prior write operation, prior memory operation. And Your Honor is very familiar with, you know, the law on consistent description in the specification helping to construe the patent and the claim terms.

I mentioned the prosecution history, Your Honor, and here's what I'm getting at. There were claims that were allowed--claim 2 is an example of that--where the allowed subject matter read before the memory read operation; very similar to the language that we have here--before the memory read operation. And there was notice of allowance. Claims were going to issue. After that notice of allowance, the patentee went back to the Patent Office and changed the claim language, changed 'before the memory read operation' to 'during one or more previous operations'. It did that for

claim 2, 3, 4, 5; did it over and over and over and over again.

And in the remarks corresponding to that amendment, the patentee said that this change, this changing from--I'll go back--'before the memory read operation' to 'during one or more previous operations', that's not a big change. It said specifically, "...have been amended to address minor issues of clarity and correct grammatical errors. No new matter has been added." The patentee there is saying that these two terms, they mean the same thing.

THE COURT: And, of course, we're not construing either of those terms.

DOCTOR ALBERT: And I will get to that, Your Honor. Very good question. I had that very same question when I was going through these materials myself.

And just to go back to the amendment, of course, the -- this change wasn't changing the scope because the Patent Office doesn't allow that. The rules for patent examination say that you can make a post-allowance amendment, but you can't change the scope. So we know that the Patent Office determined that the scope for this change would have been equivalent.

Now, we're talking about one or more previous memory operations versus one or more previous operations. Now, Netlist in this case, that was one of the terms that we were

seeking to construe. There actually is an agreement for this patent, "'one or more previous operations' means 'one or more previous memory operations'."

So getting to Your Honor's question, the claim language that we're seeking to construe here, and I'll come back to it, 'before receiving the input C/A signals corresponding'--again, these are corresponding to the memory read operation. Again, going back to that prosecution history, the memory read operation -- 'before the memory read operation' was equivalent to 'during one or more previous memory operations'.

So we have equivalent language here in the claim 'before receiving the input C/A signals corresponding to the memory read operation' when Netlist has already agreed to the Patent Office that before--I'll just go back to it--"'before the memory read operation' means 'during one or more previous operations'," which in this case Netlist has agreed in -- you see this in the joint claim construction chart "'one or more previous operations' means 'one or more previous memory operations'."

And so with that, Your Honor, I will pass the podium unless Your Honor has any questions.

THE COURT: Doesn't that equivalence depend on the context of each claim? I mean, to the extent that there's an agreement, isn't it an agreement that in those claims the claim scope wasn't altered by the different language?

DOCTOR ALBERT: Well, we can go back to the claim language itself that was purported to be equivalence, to answer your question. "'Before the memory read operation' is replaced with 'during one or more previous operations'." Again, the language that is being swapped out as equivalent starts with that memory operation.

THE COURT: What is there that is unclear about the language that you're seeking to construe? It seems very specific to me.

DOCTOR ALBERT: Yes, Your Honor.

So the ambiguity here is when this time interval is determined. And here the patent is very clear that that time interval is determined during a previous memory operation. We see it time and time and time again. And then in the prosecution history the two terms are equated as equivalence.

So we believe there should be no ambiguity; but to the extent Netlist wants to come in here and claim that's not what this means, that it means something else, then we would take issue with that.

THE COURT: All right. Thank you.

DOCTOR ALBERT: Thank you, Your Honor.

MS. ZHONG: Slide No. 41, please.

Counsel mentioned that based on the prosecution history we should be limited to construing the term to the -- the 'before' term to 'during one or more previous memory

operations'. One thing they forgot to mention in claim 15 is not one of the ones that's actually been amended. Claim 15 retained its original language--"before receiving the input command address signals corresponding to the memory read operation at the memory module control device, determining the first pre-determined amount based at least on signals received by the first data buffer." The claim is not amended.

Whatever we said about the other claims simply does not apply here. There is no reason, as Your Honor has pointed out, there is no ambiguity as to when the step needs to happen. The only limitation in the original claim is before the receiving step this happens. It can happen during one or more previous operations, and -- but it doesn't have to. And whether in that particular case the one or more previous operations constitutes what Samsung believes to be a memory operation is also not at issue here.

What Samsung really is trying to do is trying to bring in their interpretation of the memory operation into this term. That's not -- really there is no basis in either the claim language itself or the prosecution history.

So Your Honor has got it right. It should be construed by its plain and ordinary meaning, which is as the claim says.

With this we rest.

THE COURT: All right. Thank you, Ms. Zhong.

DOCTOR ALBERT: Just a very quick remark, Your

Honor. That claim 15 wasn't amended is of no moment. What matters here, Your Honor, is that during prosecution they told the Patent Office that these terms, this language was equivalence. Netlist can't take that back and say now it's not equivalence; now -- we meant it for the other claims as equivalent, but we don't mean it for this claim.

THE COURT: Why isn't their statement limited to the claims that they were talking about and the claims they were amending?

DOCTOR ALBERT: It just doesn't work that way, Your Honor. When you say to the Patent Office this language, wherever it is used, this language is the same, no -- the claims were amended to address minor issues of clarity, so this language that they took before, they changed it to something else to address minor issues of clarity, it means the same thing. Now, we find that same language in the claims that are -- in the claim that we're talking about here.

So yes, they didn't amend this specific claim, but the arguments that they made regarding the language, the common language for this claim, the claim 14 as issued, claim 15 during the prosecution, would still apply; otherwise, their statement to the Patent Office wouldn't be true.

THE COURT: Their statement to the Patent Office was that the scope of those amended claims was -- had no new matter added. Right? I fail to see how you can just assume

that the same thing would have been true for any other place that language appears.

DOCTOR ALBERT: Fair question, Your Honor, and I appreciate the insight there. The -- if you're asking the question for these claims why hasn't there been new matter added, for all these other claims that were amended why has there not been new matter added if you change the language, the only way that could be true is if those -- that new language didn't increase the scope, didn't change the scope of that claim so, therefore, that language was equivalence.

THE COURT: Okay.

DOCTOR ALBERT: And so for claim 15, we find that same language in there. Yes, they didn't make the argument regarding claim 15--very good insight, Your Honor, we appreciate that--but they did make the argument with regards to the language that is found in claim 15, as issued claim 14.

THE COURT: Except that it's not the same language.

DOCTOR ALBERT: It includes broader language, but it includes the same -- references the same memory read operation.

THE COURT: You have a tough argument, but you've made it well. Thank you.

DOCTOR ALBERT: Thank you, Your Honor. I appreciate the attention.

THE COURT: Sure.

DOCTOR ALBERT: So we'll move on now to the drive terms.

THE COURT: All right.

DOCTOR ALBERT: The core dispute with regards to these drive terms is whether the buffer as described in the '339 Patent requires switching between different data pass. Sometimes that's colloquially referred to as a fork in the road where the buffer is -- has outputs to different memory devices and it could switch between groups of memory devices, kind of like a fork in the road.

And so here we have in the proposed construction the idea is expressed by activating certain groups of memory devices while at the same time deactivating other devices. You select between one group and another group. And we're talking about a number of claims here, but they all have this drive concept, it's built into this very large claim -- you know, very large limitation. I apologize for that, Your Honor. We didn't write the claim; we just have to try to figure out what it means. But here we have this idea that you have this logic configurable to control the data path seen in claim 1. It actively drives the section of the data from a first side to a second side. So the question is, for this patent with this prosecution, what does that -- what do those drive terms mean? Does it include that fork in the road?

If you look to the '339 Patent, these data buffers are

really to accomplish two things, and the first is "to electrically couple only the enabled memory devices to the memory controller"--and so here I've got this highlighted in yellow on the left--"by using the data transmission circuits"--that's also called the buffer--"to electrically couple only the enabled memory devices to the memory controller." Now why is it doing that? It says it right there at the top--"to reduce the memory device loads seen by the system memory controller."

So their idea was that memory -- that loads were a problem, and to address that problem, they would isolate and couple -- isolate some groups of memory devices; couple other groups.

So you move onto the second function is "to electrically isolate the other memory devices which are not performing the memory operation"--and here I've got it highlighted in pink on the lower left--"and to isolate"--excuse me--"electrically isolate the other memory devices 412 from the memory controller." So this idea --

THE COURT: All of that is described as 'desirably achieved in certain embodiments'. Right?

DOCTOR ALBERT: Well, there are no other embodiments, Your Honor. And there is a dispute about that, and I will go through that.

THE COURT: Okay.

DOCTOR ALBERT: The reason, the basis, the motivation behind this coupling and isolation and switching between the two paths is to reduce the device loads. And as Your Honor is well aware that this problem to be solved is an important consideration in claim construction.

So here I have an illustration of figure 5, and I'll walk through that. That shows exactly how this is described in the patents--excuse me--in the '339 Patent. And the core concept from figure 5 is this path A and path B. Here I've got that highlighted in figure 5. The text is, "Whereby the control logic circuitry selects either path A or path B to direct the data." So you can send the data one way or you can send the data a different way. You're selecting between the paths. The selection that the patent is talking about is the selection between two different paths. And going back again, that selection is to address the problem of the device memory loads.

So going back to figure 5, it goes on, "When the control logic circuitry receives, for example, an enable A signal." So I've got this enable A signal that turns on this top A path. The top A path has a tristate buffer. It's labeled 504. That's enabled and actively drives the data value on its output, while the second tristate buffer 506--so I have marked out in red--is disabled with its in output a high impedance condition. So you have a selection between a path A and a

path B.

So here we just have that illustration. In this state the data transmission circuit allow it is data here from -- you know, from the 420 line to go up through the tristate buffer and onto Y1, which is that path A.

Here is just another figure showing the same idea. Here we have a -- the buffers are transmission circuits 416 kind of in the left middle just to the left of the highlighting, and they in path A are connected to two sets of memory devices. They're not connected to all memory devices; they're connected to two sets. So you've got this path A that connects to this we'll call ranks A and C.

Now, the patent also talks about the alternative if you want to go down path B. So if you enable B, then what you're going to have there is that the tristate buffer A that was previously activated and turned on, that is closed. Path B becomes open; path A becomes closed. And now here the data is directed to that path B terminal Y2. And that, again, is illustrated in a different figure in figure 3A. Instead of the A and C ranks being activated, the B and D ranks are activated.

So you've got this idea between a path A and a path B where some memory devices are accessed in path A and some are accessed in path B. Again, it's to implement this idea that they have this problem they are trying to solve of reducing

the load. This was their solution to the problem that the named inventors perceived.

There's a similar description on the receive side. If you -- receiving data from the memory elements into that Y1 and Y2 terminals, then the patent has a way to deal with that, and that is this multiplexer 508--I've got that highlighted--and what the patent does is it says, Well, I've got this two different inputs; I'm going to select -- selects one route to it's output. So again, we have two paths, the selection -- this concept of selection between two different paths.

And going through the patent, time and time again the patent is talking about the selection selectively allowing or inhibiting the data paths. Here we have some examples. '339 8, 41 through 53 references the module control signals by selecting or allowing the data transmission between the system memory controller, column 339--excuse me--column 10, 64 through 11:4 it's discussing these load reducing switching circuits. So again, we see that switching language to describe reducing the load by switching the paths between a path A or path B or group A and group B with this idea of this selectively switching between the paths is referenced over and over again in the patents.

Here we got it again at 11:35 to 44 discussing "data transmission circuit selectively switches between two or more

memory devices." 15:33 through 38, it switches a single data line between the memory controller and the memory device. Again, switching, switching, switching. It is talking about that concept over and over again. '339, 17:30 to 44 talks about enabling the proper data pass between the system memory controller and the targeted or selected memory devices.

That right there is enough, Your Honor. The consistent and uniform description of the patent with the idea of the switching illustrates the concept of the -- what these claims are meant to cover; what these claims do cover by enabling the data paths, according to the claim language; by driving the signal from one side to the other, according to the claim language.

But the patentee also distinguished prior art during prosecution. One of the pieces of prior art was this prior art Ellsberry, and it says, "Ellsberry does not disclose"--this is what Netlist said during prosecution--"disabling data paths in its memory bank switches. The claimed invention allows controlling of the data paths between the memory devices and the bus interface." They go on to say, "On the contrary, Ellsberry teaches away from switching the data paths in its memory banks." Again, very -- you know, this same language is repeated over and over again in the specification--switching the data paths.

So we have, again, going back to that claim language of

driving the different data paths and selecting and switching between those data paths again all comes back to reducing -- this is this solution for -- that the patentee chose to implement their -- the solution to the perceived problem of load on the system.

Now, there is a dispute about whether the specification actually does disclose an alternative embodiment, whether there is a reference to an embodiment where there isn't a switching between data paths. And Netlist makes a -- puts this in the brief. This is -- I have the language that Netlist put in their brief, and the bolded and italicized section is the same language that Netlist bolded and italicized in their brief, I believe. What they didn't do, however, is point Your Honor to the highlighted portions which I'd like to discuss.

So this language, "One or more of the data transmission circuits 416 in accordance with an embodiment of the disclosure is operatively coupled to one or more of the data lines 452 connected to one or more memory devices in each of the ranks." Now, Netlist makes a big deal about the recitation of the one saying, Well, that's the idea, there is no fork; that there can be no fork if there's only one, but that's not what -- where this sentence ends, because this sentence ends with "in each of the ranks A, B, C, D." And if I have a data line to a device, memory device, but for each

rank that's going to be multiple data lines, that's going to be multiple paths.

And it repeats it again down below, but then it specifically references figure 3 as an illustration of this concept. And Your Honor, we already saw figure 3. I showed it to you just a few minutes ago, but here is figure 3 again where I've repeated the highlighting from my earlier slides where we don't see in figure 3 a single line, a single straight line embodiment, as Netlist has coined the phrase, but a -- again, a fork-in-the-road embodiment where it goes to one group for one path and another group for another path. So this language that Netlist places so much stock into is really just an illustration again of figure 3A which shows the fork in the road.

So what does Netlist then do? Netlist then takes this concept, this single word out of context and says, Well, if it does mean one, then we can just change all of the figures to have a straight line embodiment. And this was kind of strange to us because I've never seen this in a brief, but they've taken figures and erased portions of the figures to say, *Voila*, there is your straight line embodiment; there is your no fork in the road? But what they've done is they've erased and deleted parts of the figure that describe the fork in the road. So they did it here for figure 4, they did it for figure 3, they blacked out this -- the other prong of the fork

to claim that there is now a -- not a fork in the road here. But the figures themselves describe this fork-in-the-road concept; the patent specifically describes this fork-in-the-road concept. And it's very uniform in that description about that switching between the data paths.

This was in their reply brief, a reference to 16:38 through 45. "In yet another embodiment, the multiplexer and the read buffer operations may be split over two tristate buffers, one to enable the value of Y1 and another to enable the value from Y2." And sometimes they claim the tristate buffers can operate independently and, therefore, that somehow shows the straight line embodiments.

And so what I have here on the right--I'll be very clear--this was our attempt to try to put into a picture what was described, but we didn't see a picture in the brief so this is our attempt to replace the multiplexer with these two red tristate buffers. So what I have here in red is not in the patent; it's an attempt to illustrate the replacement of the multiplexer that's described in the specification as another possibility.

And Netlist says, Well, if those two tristate buffers operate independently, then that would be a straight line embodiment because you'd have independent operation. And there's two things that are wrong with that that we saw in their reply brief is that, one, we -- the patent doesn't

describe 'independent operation' of these replacement tristate buffers; it just mentions that you can do it in -- you know, in some way. It doesn't describe 'independent operation'. Go through the patent; it's going to be nothing that describes that.

And you wouldn't do it that way because that wouldn't work. If you had these two tristate buffers and you were operating them independently, both of them are receiving memory read operations--or sorry--data from the memory devices through this Y1 and Y2, if they are single lines, you know, single straight line embodiments, what's going to happen is that that independent operation--again, not in the patent--would cause that data to merge onto the same line and crash together. That's not a product or an idea that you'd want to implement.

So the patent doesn't describe this independent operation. Netlist says that you could do it independently, but that's not described in the patent. So again, this is another thing that Netlist pointed to as somehow describing an alternative embodiment that it could be a straight line configuration or not a fork in the road, but the point here is it doesn't disclose that, and the way Netlist argues they would work would cause the system problems.

Netlist put a lot of stock into two prior ITC cases, the 1023 investigation, 1089 investigation, arguing that, Well,

for the 1023 investigation that that involved different claim language and that claim language isn't involved here; so even though the 1023 found that those claims required a fork-in-the-road implementation, that same exact claim language is not found in this case. The claim language that was issued there was this 'selectively isolate selectively allow' language. But again, that's the same language, 'selectively', that was repeated over and over in the specification but also in the prosecution in -- for this patent.

And then for the 1089 investigation, the -- that was a bit of a strange posture, Your Honor, because the ALJ decides an issue and then the commission gets to review it. And here the ALJ reviewed the fork issue, found for those claims didn't require a fork, but the commission reversed the infringement finding, and it did that on this term 'receive' which required that all of the--excuse me--that -- and built into this 'receive' concept was this idea that not all of the memory elements could receive the memory operations. In other words, some would receive it, some would not, and because the products in that case, all of them received the memory operations, there is no infringement.

So again, we have the split between some devices having some access, access -- memory operations grouped between a different set of devices. And so, again, the commission

didn't use the word 'fork in the road' to specifically implement its decision, but built into that concept, built into that decision and that concept was this fork-in-the-road idea.

But again, we're not relying -- we're not saying that these two cases are controlling. We're asking the Court to look at the facts of this case, the claim language of this case where the claim language discusses the driving of the data, activating the pass, and the prosecution history of this case which describes the selection that was used to circumvent the prior art.

THE COURT: Mr. Albert, can you go back to your slide with figure 5 from the patent; not the modified version, but the actual version?

The fork in the road that you're describing is the place where path A and path B split off at the top of figure 5 there. Is that right?

DOCTOR ALBERT: That's exactly right, Your Honor. So we'd have the two paths, path A and path B going -- and they would go through different terminals, Y1 and Y2.

THE COURT: Do you contend that you cannot drive a signal along path A without disabling path B? In other words, are you taking the position that it's not electrically possible to do that?

DOCTOR ALBERT: Well, that's -- the patent doesn't

describe a dual operation of both path A and path B.

THE COURT: I know. My question is a different question. Do you contend that you cannot drive a signal along path A without disabling path B?

DOCTOR ALBERT: Not with this circuit as disclosed in the '339. Now --

THE COURT: I don't know what that means.

DOCTOR ALBERT: Engineers are very bright, and you can certainly create a different circuit with a different disclosure that could drive different pins at the same time, but that's not the disclosure or the circuit we are discussing here. The disclosure for this circuit would be in either path A or path B.

THE COURT: All right. And my question is do you contend that you cannot drive a signal along path A of this circuit without disabling path B.

DOCTOR ALBERT: Yes, that is the way that the patent describes the path A path B operation.

THE COURT: All right. So you're answering about your interpretation of the disclosure in the specification and I'm asking about the figure as it appears there, but anyway --

DOCTOR ALBERT: To put a finer point on that, Your Honor--I don't mean to duck your question--the -- if you look to see, there is a control going into the tristate buffers

that we have -- you know, 430 goes into 502, and then that controls the different tristate buffers. The way that this circuit operates, the way that this circuit -- this particular circuit with this control scheme operates is that you would not be able to drive it onto path A and path B because of that control circuit. Now, if we took out parts of the figure where there wasn't that control and put something else in, then, you know, maybe it might be possible, but I'm -- we're not seeing it with this control circuit.

THE COURT: All right. Mr. Albert, let me go ahead and take the morning recess now. We'll come back and hear if you have additional remarks and then the response.

DOCTOR ALBERT: Thank you, Your Honor.

THE COURT: Thank you.

(Brief recess.)

THE COURT: Thank you. Please be seated.

Mr. Albert, do you have anything further on this term?

DOCTOR ALBERT: Nothing further on this term, Your Honor.

THE COURT: All right. Thank you, sir.

MS. ZHONG: So the counsel has argued at length focusing on the full rank embodiment of the '339 Patent. What the counsel fails to mention is that the specification is very clear. Even though the description is with respect to four ranks, embodiments with less than four ranks, including two

ranks per memory record 402, 402 prime may be employed. And why is that important? It is important because if you only have two ranks, a single path is sufficient.

For example, if we look at figures 3A, there are two 452 lines--one 452 connecting the purple colored 416, which is a data buffer, to ranks A and C. There is a second one that we have grayed out that's connecting data buffer 416 to the two other ranks B and D. But if you only have two ranks, A and C, a single pass is needed, so there is no need for the fork in the road. That's a straight line configuration there. And if we don't have a second line, disabling the second line just doesn't make any sense. And the claim does not require that there be four ranks with two different paths.

And why do we know that the two ranks is actually contemplated by the invention? Let's go back to what the counsel said. The purpose of this invention is load reduction. If Your Honor take a look at figure 2A, figure 2A as described in columns 5, lines 44 to 64, that's a prior art configuration with two ranks. And in particular, in column 5, lines 45 to 48, the inventors described that with respect to the two-rank operation there is a load problem. Sorry. I got the lines wrong. The lines that's relevant to the load reduction starts actually column 5, lines 59.

So with respect to two-rank, they say, "Therefore, during a write operation, the system memory controller 220 sees all

the memory devices 212 as its load, the other data lines 250." That is, it sees two ranks of memory modules.

And what does our invention do? Regardless of the number of ranks, the invention allows you to -- the memory controller to see a single rank. Where is that disclosed? That's disclosed, for example, in column 14, starting at line 59. It says, "To reduce a memory device load seen by the system memory controller 420, e.g., during a write operation, the data transmission circuit 416 of certain embodiment is configured to be recognized by the system memory controller 420 as a single memory load."

So even for two-rank, it used to be in a prior art, the memory module sees two ranks of memories and now it sees as a single load, a single rank. So there is load reduction there for two-rank. And for the two-rank, as I show on screen here, a single line is sufficient. You don't need to have a second -- what they call the fork in the road. Without the fork in the road, disabling the second path, as they suggest, is just not justified.

Now, I understood that counsel said during prosecution we were talking about selecting or switching the pass on and off. I think it's a misunderstanding of what we were actually saying.

So let's look at column -- slide No. 10.

The argument is actually saying the data passing

Ellsberry switches 206/208 are opened by default. What our claim is really requiring is that that particular path is turned on during a specific time period, and when the data passes on the operation -- the write data or read data is passed on the data pass are then turned off. So when the counsel is talking about switching on, selecting on and off, they're not talking about switching between different paths; they're talking about a single path A is switched on during specific time period. So they're talking about temporal turning on and off, not physical, spatial turning on from -- switching from one pass to another. So that was a complete misrepresentation of what we argued during prosecution.

With respect to Your Honor's question regarding figure No. 5 --

Maybe slide No. 18, please.

Figure No. 5, Your Honor asked whether in this particular embodiment it has to be the case that the second pass is turned off. Our understanding is that it doesn't have to be. It can be turned on as in prior art. You can use, for example, a technique called data masking for the write path and the data can be sent and only be selected -- only received -- the useful data is only received by the memory device that's intended to receive the data where the write -- so the data pass can be open, like both can be on at the same time.

THE COURT: Would that serve the goals of the

invention in this patent?

MS. ZHONG: So if you do that, I think you do see some load reduction, not as much, so instead of, like, reducing the load from four loads to one load, you may be reducing it from four loads to two loads.

THE COURT: All right.

MS. ZHONG: Okay. Does Your Honor have additional questions? If not, we will rest.

THE COURT: I think I understand your position on it. Thank you.

Mr. Albert, if you want to respond, you may.

DOCTOR ALBERT: Thank you, Your Honor.

Just a couple of points here.

With regards to the point about the possibility of a two-rank system and the argument that, Well, the patent in this invention could have been implemented not using this fork in the road with two ranks, I kept hearing 'could have', 'didn't have to be', 'could have been implemented'. That's not what the specification says. When the specification implements this invention, it is always with that fork in the road. And in order to be able to concoct a straight line embodiment without a fork in the road, Netlist has had to alter the figures in the patent, which is telling.

So this idea that you could have done something differently, that -- Your Honor, that is the case with every

single patent that falls in front of you--that you could have done things differently. The question before this Court is what was disclosed in this specification and this prosecution history. And this prosecution history, again, Netlist in its briefing, you know, put big emphasis on that 'switching' language in the ITC case, and that same language is found in the prosecution history--switching of the data lines.

So with that, unless Your Honor has any further questions.

THE COURT: You know, Mr. Albert, one of the problems that this proposed construction faces is the fact that you're construing one word with what is probably 200 words. I am -- I don't know that I've ever seen a more elaborate proposed construction for a single term.

DOCTOR ALBERT: And I'm glad Your Honor asked that question because, unfortunately, this is a byproduct of repeated litigation by Netlist. Netlist asserted these patents in this family against similar technology, was found not to infringe, got continuations repeated, and there's been this serial continuing prosecution for these patents to make longer and longer claims, more complicated claims for this simple idea that there is a fork in the road.

So what we have here is not just the word 'drive' that's being construed, Your Honor, because it's not just 'drive' in the abstract; it's 'drive' -- let me just take claim 1, for

example. This whole phrase, this complicated phrase that Netlist has put in their patent all goes to this concept of the fork in the road of this switching. It starts with the buffer, including the logic configurable to control the data path. Again, we saw in the specification that that path A control and that path B control, splitting the two paths, the path that the data would ultimately follow and switching between the one group of memory versus the other group of memory, that's built into this phrase as well as other portions of this claim.

It goes on to say that the data path is enabled. Enabled. So we're enabling and disabling data paths. So we're -- we have that logic to control the data path, just like that path A and path B embodiment that we saw in the spec that was repeated over and over and over again, the only way that the control is described.

And then it talks about driving the data from one side of the buffer to the other side of the buffer. And again, the only way the patent describes that driving, that -- from one side to the other is with this fork in the road. You drive it from, you know, one group or the other group.

And then it talks about the -- again, the tristate buffers. I showed those to you in figure 5 where you enable path A, you are enabling the path A tristate buffer and correspondingly disabling because of that control circuitry

the path B.

So it's not just a single word that's been construed, Your Honor; it's the entire collection of this language. Very complicated, we understand, but it's really results of this continuing serial application that Netlist has undergone.

THE COURT: All right. Thank you, Mr. Albert.

DOCTOR ALBERT: With that, we will rest on the papers for 'module controller', the next term, Your Honor.

THE COURT: All right.

MR. SHEASBY: Your Honor, Mr. Tezyan was going to argue that term, and I would like to represent to the Court that he was awesome when we went through it yesterday and it would have been his first argument. So if we could get judicial notice of that, I would appreciate it.

THE COURT: All right. We'll direct that his remarks be placed in the record.

MR. SHEASBY: Can I have the elmo, Madam Courtroom Deputy?

So this is the last term that we are arguing, and the attention is -- and I appreciate the Court's indulgence by not just saying 'plain and ordinary meaning', but actually wading into the dispute. And I think everyone agrees, if you go back and look at the specification, the portion of the specification that guides this is column 50, lines 60, *et seq*, to column 16, lines 5. And the only point I will make, Your

Honor, is in that section I have highlighted the relevant time period. The latency is not just the moment that it starts; it's also the moment that it stops as well.

In the construction as given in a time period where the start of -- wherein the start of the time period depends on at least the latency parameter, it would create significant difficulty in applying the claim during the infringement phase of the case if the back end of the latency period was not defined.

And so consistent with column 15, we would ask that the language -- in fact, we'd be comfortable with the language directly from there where it says "from the moment the memory controller starts to it stops". If we could just use that exact language, we would appreciate it, because it is going to create confusion at the time period in the subsequent case. And I think that a period of time has a beginning and an end. I don't think that's in dispute. And the latency controls both the beginning and the end of that time period, and we'd like to make that clear based on the specification that I just read, Your Honor.

THE COURT: All right.

DOCTOR ALBERT: Admittedly, Your Honor, I don't know what to make of that. I don't know what's being proposed by Netlist at this point, and I don't know what the dispute is given the statements.

THE COURT: It's my understanding of their statement that they are still seeking duration, but that they feel they can get there if the construction includes both the start and the end.

DOCTOR ALBERT: And here, Your Honor, perhaps a little bit of clarity as to our understanding would be helpful here.

So if you look at the claim language, 'time period in accordance with a latency parameter', Your Honor's construction follows that 'a time period wherein the start of the time period depends on at least a latency parameter'. That was different than Netlist had sought, which is the start and duration depending on a latency parameter. So my understanding of the tentative was that the 'and the duration' was excluded from the construction.

THE COURT: That was a correct understanding.

DOCTOR ALBERT: And so as Your Honor distinctly tuned into here, the specification discusses latency parameter, discusses latency, and talks about latency is a delay time--right?--something that elapses between one event and another. And Netlist's original construction -- I don't quite know if that's what their getting at right now, but their original construction was not just a delay time--which, you know, you could also call that a duration, a duration of a delay--they wanted a construction of a latency parameter to

include the duration of delay--you know, that delay time--but also a second duration, and that's where we have issue with.

So we -- Your Honor correctly and keenly tuned into the real issue here that latency is that delay time, as is described in the specification, and the -- it requires no further construction than that. The patent itself says that this is a known thing in the field. Patent -- I couldn't tell whether counsel was saying that the specific description in the patent was an expressed definition that changed the meaning in the field, that differed from the meaning in the field, but the patent acknowledges that this is a known parameter and then goes on to describe it as a delay, and just like Your Honor's construction of a time period where the start of the period depends at least on a latency parameter.

THE COURT: I think what we're really construing is what 'time period in accordance with' means here, because I agree with you that there seems to be agreement about what the latency parameter itself is.

DOCTOR ALBERT: And the original dispute that -- as I understood it from the briefing, Your Honor, was Netlist seemed to be trying to redefine the term 'in accordance with', which didn't argue in the brief that 'in accordance with' had a very specific meaning, but that was the implication of their argument.

You know, based on the Court's construction, you know, we

don't have any further points here.

I would just go on to say, Your Honor, that, you know, there is an IPR outstanding on this issue, as Your Honor may know. After the briefing finished, the institution decision came out instituting on all claims. And the Patent Office sided with Samsung's construction here, which would be consistent with Your Honor's construction that it -- the time period of that starts based on the latency parameter.

So with that and, you know, barring further clarification from Netlist counsel as to whether they mean something other than what Your Honor has written down, we have no further points here.

THE COURT: All right. Thank you, Mr. Albert.

MR. SHEASBY: Your Honor, I wrote down what counsel said is he, quote, elapses between one time and another as the period, and we agree with that. What we're trying to make clear, and we understand that our proposed construction had issues with sort of second latency period or things like that, that was not our intention. Our point is that the latency period is between two moments. It's not just -- it doesn't just control when the period -- the latency parameter doesn't just control when the period starts; it also controls where the period ends, of necessity. And I think if 15, line 61 through 65, which is the same passage that they quote in their brief--they just allied part of that--makes it clear that the

period from when it starts to when it ends, and that's the only request we would make consistent with the specification, Your Honor.

THE COURT: Well, if the latency parameter is clear, why doesn't 'using it to set the start time' resolve the whole thing?

MR. SHEASBY: Because it -- using it -- they will take the position that 'using a latency parameter to set the start time doesn't mean that the latency parameter controls the end time. So they -- their position technically will be that they're not necessarily linked, they're not inherently linked; you can start one -- you can have it start it but not have it when it ends.

And so our position is in the specification to latency period, in column 15, lines 61 through 65 makes clear that the latency period is not just the beginning, it's the end. And I'll read that into the record. "The column addressed strobe latency"--that's what we're referring to here; I think both parties agree on that--"is the delay time which elapses between the moment the memory controller informs the memory module to access a particular column in a selected rank or row and the moment the data from the particular column is on the output pins of the selected rank or row."

And so the latency parameter controls the entire period--not just when it starts, but when it ends. And

Samsung will take the position that it's not inherent, that when it starts -- controlling when it starts means you're controlling when it ends.

THE COURT: All right.

MR. SHEASBY: Thank you, Your Honor.

THE COURT: Thank you.

DOCTOR ALBERT: Your Honor, as I understand, Netlist's position is just a rephrasing of their prior construction a time period with the start of the time period and the duration of the time period depends on at least the latency parameter.

THE COURT: Mr. Albert, can you describe your position through the use of figure 6? I saw that you had a slide on that a little earlier.

DOCTOR ALBERT: Yes. So figure 6 is instructive, Your Honor, because there are -- the patent describes 'latency', and with regards to figure 6, the patent also describes these time periods 601, 602, 603. The patent uses different language for that -- to describe latency and the periods. It doesn't link the two together like Netlist's construction is now linking.

Latency is just a delay of time. It's found in their own dictionary definition they cited. It's a delay time. We agree it's a delay time. But that's not the crux of the issue, because the crux of the issue is that the -- as Your

Honor pointed out with Netlist's -- the dispute really seems to be now is the language period 'in accordance with', and what does that mean; how narrow is that term. And Your Honor correctly pointed out that 'in accordance' means it could be dependent on the start time.

Now, does 'in accordance' mean, as Netlist seems to now imply, that every variable has to be defined for that period for 'in accordance'? No. That's not what 'in accordance' means. And if you actually look at the patent, 'in accordance with' is used throughout the patent to describe various things, including some of the figures, which don't have all of the description from the specification. 'In accordance with' is -- in the patent is used as a general term. It could be used as 'depend on', just like Your Honor has found.

So with that, with the evidence in the record, we believe Your Honor has gotten this one correct.

THE COURT: The claim language in claim 1 that talks about the latency parameter refers to the path -- data path being enabled for a first time period in accordance with the latency parameter. So is your understanding of the plain meaning of that that the latency parameter determines when it starts, but the claim does not dictate when that enablement of the path ends?

DOCTOR ALBERT: Yes, Your Honor, that would be sufficient. And that's -- again, that's exactly what the

Patent Office just found in its institution decision regarding these claims.

THE COURT: All right.

DOCTOR ALBERT: And I can put that language up, Your Honor. "On this record we are sufficiently persuaded by Petitioner's argument that enabling the data path for a time period that starts based on the latency parameter. The patent owner does not sufficiently address whether claim language require latency to relate to the duration of the time periods during which the data is driven rather than the start of the time period."

THE COURT: Thank you.

MR. SHEASBY: And I'll just make the point that the duration thing is obviously -- the use of the word 'duration' is obviously inartful, but I think if you look at the claim language, the latency parameter is controlling the first time period and that first time period is the beginning -- includes the beginning and end of the period.

So I think from the claim language itself, it's required that the latency parameter control both the first and -- the beginning and the end. And I'll read that into the record. "A latency parameter to actively drive the respective byte-wise section of the end bit wide write data associated with the memory operation from the first side to the second side during the first time period." From the first side to

the second side, from the beginning, the moment of the beginning to the moment at the end, Your Honor. Thank you.

THE COURT: And is it your understanding of latency, as used here, that it's talking about something that's inherent in the system; some number of clock cycles that is programmed in?

MR. SHEASBY: Yes. So it's not inherent in the system. You have to program it in. Or it's based on -- I think the tristate buffer is what actually does it, which actually delays it so that you get -- you're delaying both the start and the end so that you're not having a collision with -- in figure 6 it's depicting it in one cycle, but there's no magic to it being in just one cycle. The write process could take two cycles, for example, and when it took two cycles you'd want to make sure that the alternative tristate buffer didn't start until the end; not just that it didn't start after the beginning.

THE COURT: All right.

MR. SHEASBY: That's why it says from the moment -- this is not -- that's right. This is not active. The language they put up 15:61 through 66 says it--"from the moment the memory controller informs the memory module to begin the process until the moment the process is completed." That's the whole point--the latency controls that entire period.

THE COURT: All right. Thank you.

DOCTOR ALBERT: Just one final point here.

It seems like Netlist is now arguing for an express definition of 'latency parameter' from the specification, but I'll point out that the language that they're pointing to is not latency parameter generally; it's a specific type of latency, column address strobe latency, which is a different term. That is a -- that's different language, different term. 'Latency' can be backed out from here. It is a delay time.

THE COURT: So do you contend that when the claim refers to 'latency parameter', it's not referring to the 'column address strobe latency' that's described in the specification?

DOCTOR ALBERT: This is one example of 'latency', and the examples of -- the example that has been chosen here for 'latency' is a particular type of latency--'column address strobe'.

Now, Netlist has offered other evidence about what 'latency' means that is different that's not dependent on this 'column address strobe latency', but to read this specific example of 'latency', a term that is known, into this construction, we don't believe that's proper. But the general idea of 'latency' is known. We believe that plain meaning controls. We also see that Your Honor's construction is consistent with that.

THE COURT: All right.

MR. SHEASBY: And I'll just point out for the record, this is Docket 82, page 29, it's 15:61 through 16:6, that Samsung in briefing used to describe the meaning of 'latency', and that's the CAS latency passage that is up on the screen right now. So I believe there has been some drift between what was represented on papers and what was just represented now.

Thank you, Your Honor.

THE COURT: All right. Thank you.

Well, I take it there are no further arguments on these terms. Is that right?

MR. McKEON: Nothing from Samsung, Your Honor. Thank you.

THE COURT: All right.

MR. SHEASBY: Nothing from the Plaintiff, Your Honor. Thank you for your time today.

THE COURT: All right. The arguments have been helpful, and I will further consider them and try to get out a claim construction order promptly.

So with that, thank you. And we're adjourned.

(End of hearing.)

I HEREBY CERTIFY THAT THE FOREGOING IS A CORRECT TRANSCRIPT FROM THE RECORD OF PROCEEDINGS IN THE ABOVE-ENTITLED MATTER. I FURTHER CERTIFY THAT THE TRANSCRIPT FEES FORMAT COMPLY WITH THOSE PRESCRIBED BY THE COURT AND THE JUDICIAL CONFERENCE OF THE UNITED STATES.

S/Shawn McRoberts 11/07/2022

_____DATE_____
SHAWN McROBERTS, RMR, CRR
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